REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

FIGs. 2A-2F have been designated as "Prior Art". This should obviate the rejection thereto.

The informalities to the claims have been obviated by the amendment herein.

In addition, the rejections under §112 have been obviated by the rewritten claims that are submitted herewith.

Claims 60-62 and 72-85 stand rejected under 35 USC 103(a) as allegedly being unpatentable over the admitted prior art of FIGs. 2A-2B in view of Tang. In response, claims 60, 77, and 78 have been canceled. Claims 61 and 73-76 are amended, and new claims 86 and 87 are added to replace the canceled claims. It is respectfully suggested that this obviates the rejection.

As now claimed, the invention defines a semiconductor island with silicon provided over a substrate. A source region, a drain region, and a channel region are provided. Because of this operation, the layer with metal is divided over the substrate under an interlayer dielectric and is connected with one of the source and drain regions. This region further includes a contact hole provided over the metal layer in the dielectric. Because of this, it is not necessary to provide a contact hole over the source region and drain region in the

interlayer dielectric. Therefore, the area of the semiconductor island can be reduced. This reduced area semiconductor island can improve the circuit arrangement. Moreover, because the contact hole is provided over the metal layer, contact failure can be reduced.

The invention of the new claims 86 and 87 includes a source region and drain region with a metal silicide. This allows the resistivity of the circuit portions with TFTs to be reduced.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "Version With Markings To Show Changes Made".

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice of allowance is hence respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 3/6/01

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

In the Claims:

Claim 60 (first occurrence) and claims 77-78 have been canceled.

Claims 86 and 87 have been newly added.

Claims 61, 73, 74, 75, and 76 have been amended as follows.

(Amended) [60.] 61. [An electro optical] A display device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided [over] in said [substrate] semiconductor island;

a channel region provided [over] in said [substrate] semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate [interconnect] interconnection provided in a same layer as said gate electrode;

a [metal] layer comprising [titanium] metal provided over said substrate and being in direct contact with said gate

[interconnect] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said [metal] layer comprising metal;

a contact hole provided over said [metal] layer comprising metal in said interlayer dielectric; and

a top layer [interconnected] interconnection comprising aluminum provided over said interlayer dielectric and connected with said [metal] layer comprising metal through said contact hole.

73. (Amended) A semiconductor device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided [over] in said [substrate] semiconductor island;

a channel region provided [over] in said [substrate] semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate [interconnect] interconnection provided in a same layer as said gate electrode;

a [metal] layer comprising [titanium] metal provided over said substrate and being in direct contact with said gate [interconnect] interconnection and being connected with one of said source region and said drain region, said [metal] layer comprising metal being connected with said gate [interconnect] interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said [metal] layer comprising metal;

a contact hole provided over said [metal] layer comprising metal in said interlayer dielectric; and

a top layer [interconnect] interconnection comprising aluminum provided over said interlayer dielectric and connected with said [metal] layer comprising metal through said contact hole.

74. (Amended) A semiconductor device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided [over] in said [substrate] semiconductor island;

a channel region provided [over] in said [substrate] semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate [interconnect] interconnection provided in a same layer as said gate electrode;

a [metal] layer comprising [titanium] metal provided over said substrate and being in direct contact with said gate [interconnect] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode and said [metal] layer comprising metal;

a contact hole provided over said [metal] layer comprising metal in said interlayer dielectric; and

a top layer [interconnect] interconnection comprising aluminum provided over said interlayer dielectric and connected with said [metal] layer comprising metal through said contact hole.

75. (Amended) A semiconductor device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided [over] in said [substrate] semiconductor island;

a channel region provided [over] in said [substrate] semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate [interconnect] interconnection provided in a same layer as said gate electrode;

a [metal] layer comprising [titanium] metal provided over said substrate and being in direct contact with said gate [interconnect] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode and said [metal] layer comprising metal;

a contact hole provided over said [metal] layer comprising metal in said interlayer dielectric; and

a top layer [interconnect] interconnection comprising aluminum provided over said interlayer dielectric and connected with said [metal layer comprising metal through said contact hole.

76. (Amended) A semiconductor device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided [over] in said [substrate] semiconductor island;

a channel region provided [over] in said [substrate] semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

a gate [interconnect] interconnection provided in a same layer as said gate electrode;

a [metal] layer comprising [titanium] metal provided over said substrate and being in direct contact with said gate [interconnect] interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said [metal] layer comprising metal;

a contact hole provided over said [metal] layer comprising metal in said interlayer dielectric; and

a top layer [interconnect] interconnection comprising aluminum provided over said interlayer dielectric and connected with said [metal] layer comprising metal through said contact hole.

Please add the following new claims.

86. (New) A display device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnection provided in a same layer as said gate electrode;

a layer comprising said metal provided over said substrate and being in direct contact with said gate interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.

87. (New) A semiconductor device comprising:

a substrate;

a semiconductor island comprising silicon provided over said substrate;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a gate interconnection provided in a same layer as said gate electrode;

a layer comprising said metal provided over said substrate and being in direct contact with said gate interconnection and being connected with one of said source region and said drain region, said layer comprising said metal being connected with said gate interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.